

Remarks

The final Office Action dated May 18, 2009, maintains the following: a rejection of claims 1, 5 and 7 under 35 U.S.C. § 102(b) over Thuringer (U.S. Patent No. 6,498,404); a rejection of claims 2-4 under 35 U.S.C. § 103(a) over the ‘404 reference in view of the Patterson reference (“Computer Architecture: A Quantitative Approach”); and a rejection of claim 6 under 35 U.S.C. § 103(a) over the ‘404 reference. Claims 8-14 are noted as being substantially similar to claims 1-7 and are rejected. In this discussion set forth below, Applicant does not acquiesce to any rejection or averment in this Office Action unless Applicant expressly indicates otherwise.

Applicant maintains the traversals of the § 102(b) and § 103(a) rejections because the cited Thuringer ‘404 reference either alone or in combination with the Patterson reference lacks correspondence. The Examiner continues to overlook the fact that the asserted references do not teach the claimed invention “as a whole” (§ 103(a)) including aspects such as pairs of processing signals coming into and out of respective ones of the processing circuits, and “a current drawing circuit … controlled by the activity monitor circuit to draw a cloaking current controlled by the combined activity signal, so that power supply current variations dependent on the secret information are cloaked” In contrast, at page 4, the Examiner does not even argue that the ‘404 reference teaches a load circuit which is controlled by the activity monitor circuit in any manner, no less as further claimed by Applicant “power supply current variations dependent on the secret information are cloaked” Apart from alleging that Applicant’s claim language is considered “broad”, the Examiner has not attempted to provide any substantive explanation regarding this and other distinctions, after previous requests by Applicant, regarding how the ‘404 reference could be interpreted to provide such alleged correspondence.

Applicant further maintains the traversal of the § 103 rejection of claims 2-4 because the cited references teach away from the Office Action’s proposed combination. Consistent with the recent Supreme Court decision, M.P.E.P. § 2143.01 explains the long-standing principle that a § 103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main (‘404) reference—the rationale being that the prior art teaches away from such a modification. *See KSR*

Int'l Co. v. Teleflex, Inc., 127 S. Ct. 1727, 1742 (2007). Applicant explained that the combination would render the invention inoperable because the '404 reference is an asynchronous circuit, whereas the Patterson teaching (relied upon) in the Office Action is a synchronous approach; the two approaches are inoperable as asserted. Under M.P.E.P. § 2143.01, the rejections cannot be maintained. In response to this argument, the Examiner admits that vague teaching from the '404 reference is being relied upon to maintain this rejection – again without any further explanation.

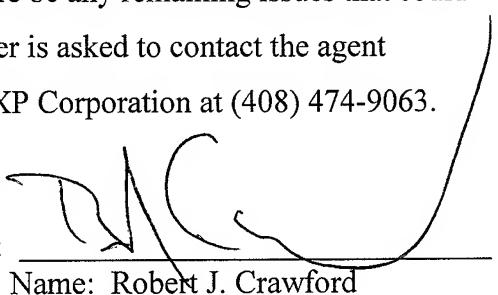
Without further explanation, the record indicates that, at best, the Examiner's § 103 rejections are based solely on "obvious to try" arguments. Such a rejection, however, has been reviewed and assessed adversely by the *In re Kubin* court which explains that the "obvious to try" standard may not be applied where one would have "to vary all parameters or try each of numerous possible choices until one possibly arrived at a successful result, where the prior art gave either no indication of which parameters were critical or no direction as to which of many possible choices is likely to be successful." *In re Kubin* (Fed. Cir. April 3, 2009), interpreting KSR. See also M.P.E.P. § 2143(E), and *Gillette Co. v. S.C. Johnson & Son, Inc.*, 919 F.2d 720, 725 (Fed. Cir. 1990). Here, the skilled artisan would clearly recognize that the statement relied upon from the '404 reference is not only vague but it is illogical and erroneous as no conventional digital circuit can process signals independent of synchronous/asynchronous construction of the logic. This overly-broad thinking is exactly that which has been rejected by the *In re Kubin* Court as giving "either no indication of which parameters were critical or no direction as to which of many possible choices is likely to be successful."

Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063.

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

CUSTOMER NO. 65913

By: 

Name: Robert J. Crawford
Reg. No.: 32,122
651-686-6633
(NXPS.589PA)